In the Claims

1. (Previously Presented) A method for operating a memory cell, comprising:

applying a negative voltage to a gate of a PMOS transistor formed in an n-type well, wherein the PMOS transistor includes:

a first source/drain region;

a second source/drain region, wherein the first and the second source/drain region include source/drain regions having a work function greater than 4.1eV;

a channel located between the first and the second source/drain regions;

a gate opposing the channel, wherein the gate includes a gate having a work function greater than 4.1eV;

a gate insulator separating the gate from the channel, wherein the gate insulator is less than 20 Angstroms thick;

coupling the n-type well to a positive voltage which is less than a power supply voltage; and

reading a charge level of a storage device, wherein the storage device includes a first and a second storage node, the first and the second storage nodes having a work function greater than 4.1eV.

2. (Original) The method of claim 1, wherein coupling the n-type well to a positive voltage which is less than a power supply voltage achieves lower tunneling charge leakage from the gate.

3. (Previously Presented) A method for operating a memory cell, comprising:

applying a negative voltage to a gate of a PMOS transistor formed in an n-type well, wherein the PMOS transistor includes:

a first source/drain region;

a second source/drain region, wherein the first and the second source/drain region include source/drain regions having a work function greater than 4.1eV;

a channel located between the first and the second source/drain regions;

a gate opposing the channel, wherein the gate includes a gate having a work function greater than 4.1eV;

a gate insulator separating the gate from the channel, wherein the gate insulator is less than 20 Angstroms thick;

coupling the n-type well to a voltage which is equal to a power supply voltage; and

reading a charge level of a storage device, wherein the storage device includes a first and a second storage node, the first and the second storage nodes having a work function greater than 4.1eV.

4. (Original) The method of claim 3, wherein coupling the n-type well to a voltage which is equal to a power supply voltage achieves lower tunneling charge leakage from the gate and lower junction leakage from the second source/drain region and storage device when the storage device is not charged.

5. (Previously Presented) A method for operating a memory cell, comprising:

applying a negative voltage to a gate of a PMOS transistor formed in an n-type well, wherein the PMOS transistor includes:

a first source/drain region;

a second source/drain region, wherein the first and the second source/drain region include source/drain regions having a work function greater than 4.1eV;

a channel located between the first and the second source/drain regions;

a gate opposing the channel, wherein the gate includes a gate having a work function greater than 4.1eV;

a gate insulator separating the gate from the channel, wherein the gate insulator is less than 20 Angstroms thick;

coupling the n-type well to a voltage which is greater than a power supply voltage; and

reading a charge level of a storage device, wherein the storage device includes a first and a second storage node, the first and the second storage nodes having a work function greater than 4.1eV.

6. (Currently Amended) The method of claim 5, wherein coupling the n-type well to a positive voltage which is greater than a power supply voltage results in less junction leakage at the first and second source/drain regions.

7. (Previously Presented) A method for operating a memory cell, comprising:

activating a gate of a PMOS transistor formed in an n-type well, wherein the PMOS transistor includes:

a first p-doped source/drain region;

a second p-doped source/drain region, wherein the first and the second source/drain region include source/drain regions formed from a material having a work function greater than 4.1eV;

a channel located between the first and the second source/drain regions;

a gate opposing the channel, wherein the gate includes a gate formed from a silicon compound having a work function greater than 4.1eV; and

a gate insulator separating the gate from the channel,

applying a voltage to the n-type well; and

reading a charge level of a storage device coupled to the second source/drain region.

8. (Original) The method of claim 7, wherein applying the voltage to the n-type well includes applying a voltage lower than a supply voltage to the n-type well.

9. (Original) The method of claim 7, wherein applying the voltage to the n-type well includes applying a voltage equal to a supply voltage to the n-type well.

10. (Original) The method of claim 7, wherein applying the voltage to the n-type well includes applying a voltage higher than a supply voltage to the n-type well.

11. (Original) The method of claim 7, wherein the silicon compound includes a silicon compound chosen from a group consisting of p-doped silicon carbide and p-doped silicon oxycarbide.

12. (Previously Presented) A method for operating a memory cell, comprising:

activating a gate of a PMOS transistor formed in an n-type well, wherein the PMOS transistor includes:

a first p-doped source/drain region;

a second p-doped source/drain region, wherein the first and the second source/drain region include source/drain regions formed from a material having a work function greater than 4.1eV;

a channel located between the first and the second source/drain regions;

a gate opposing the channel, wherein the gate includes a gate formed from a metal having a work function greater than 4.1eV; and

a gate insulator separating the gate from the channel,

applying a voltage to the n-type well; and

reading a charge level of a storage device coupled to the second source/drain region.

13. (Original) The method of claim 12, wherein applying the voltage to the n-type well includes applying a voltage lower than a supply voltage to the n-type well.

14. (Original) The method of claim 12, wherein the metal includes a metal chosen from a group consisting of cobalt, nickel, ruthenium, rhodium, palladium, iridium, platinum, and gold.

15. (Previously Presented) A method for operating a memory cell, comprising:

activating a gate of a PMOS transistor formed in an n-type well, wherein the PMOS transistor includes:

a first p-doped source/drain region;

a second p-doped source/drain region, wherein the first and the second source/drain region include source/drain regions formed from a material having a work function greater than 4.1eV;

a channel located between the first and the second source/drain regions;

a gate opposing the channel, wherein the gate includes a gate formed from a metal nitride having a work function greater than 4.1eV; and

a gate insulator separating the gate from the channel,

applying a voltage to the n-type well; and

reading a charge level of a storage device coupled to the second source/drain region.

16. (Original) The method of claim 15, wherein applying the voltage to the n-type well includes applying a voltage equal to a supply voltage to the n-type well.

17. (Original) The method of claim 15, wherein the metal nitride includes a metal nitride chosen from a group consisting of titanium nitride, tantalum nitride, tungsten nitride, and molybdenum nitride.

18. (Currently Amended) A method for operating a memory cell, comprising:

activating a gate of a PMOS transistor formed in an n-type well, wherein the PMOS transistor includes:

a first source/drain region;

a second source/drain region, wherein the first and the second source/drain region include source/drain regions formed from a first doped semiconductor material having a work function greater than 4.1eV;

a channel located between the first and the second source/drain regions;

a gate opposing the channel, wherein the gate includes a gate formed from a second doped semiconductor material having a work function greater than 4.1eV; and

a gate insulator separating the gate from the channel[[,]];

applying a voltage to the n-type well; and

reading a charge level of a storage device coupled to the second source/drain region.

19. (Original) The method of claim 18, wherein applying the voltage to the n-type well includes applying a voltage higher than a supply voltage to the n-type well.

20. (Currently Amended) The method of claim 18, wherein the first doped semiconductor material and the second doped semiconductor material include p-doped semiconductor material.

21. (Original) The method of claim 18, wherein the second doped semiconductor material includes a doped semiconductor material chosen from a group consisting of p-doped silicon, p-doped germanium, p-doped silicon germanium, p-doped gallium nitride, and p-doped gallium aluminum nitride.

Conclusion

Claims 6, 18, and 20 have been amended for clarity. It is respectfully submitted that these changes do not introduce new matter, and the claims are allowable without further search or consideration. Therefore, entry is appropriate under Rule 312, and is respectfully requested.

Respectfully submitted,

LEONARD FORBES ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6944

Date 10/5/05 By ______________________
David C. Peterson
Reg. No. 47,857

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Eric Olson
Name

Signature